

FIG.1

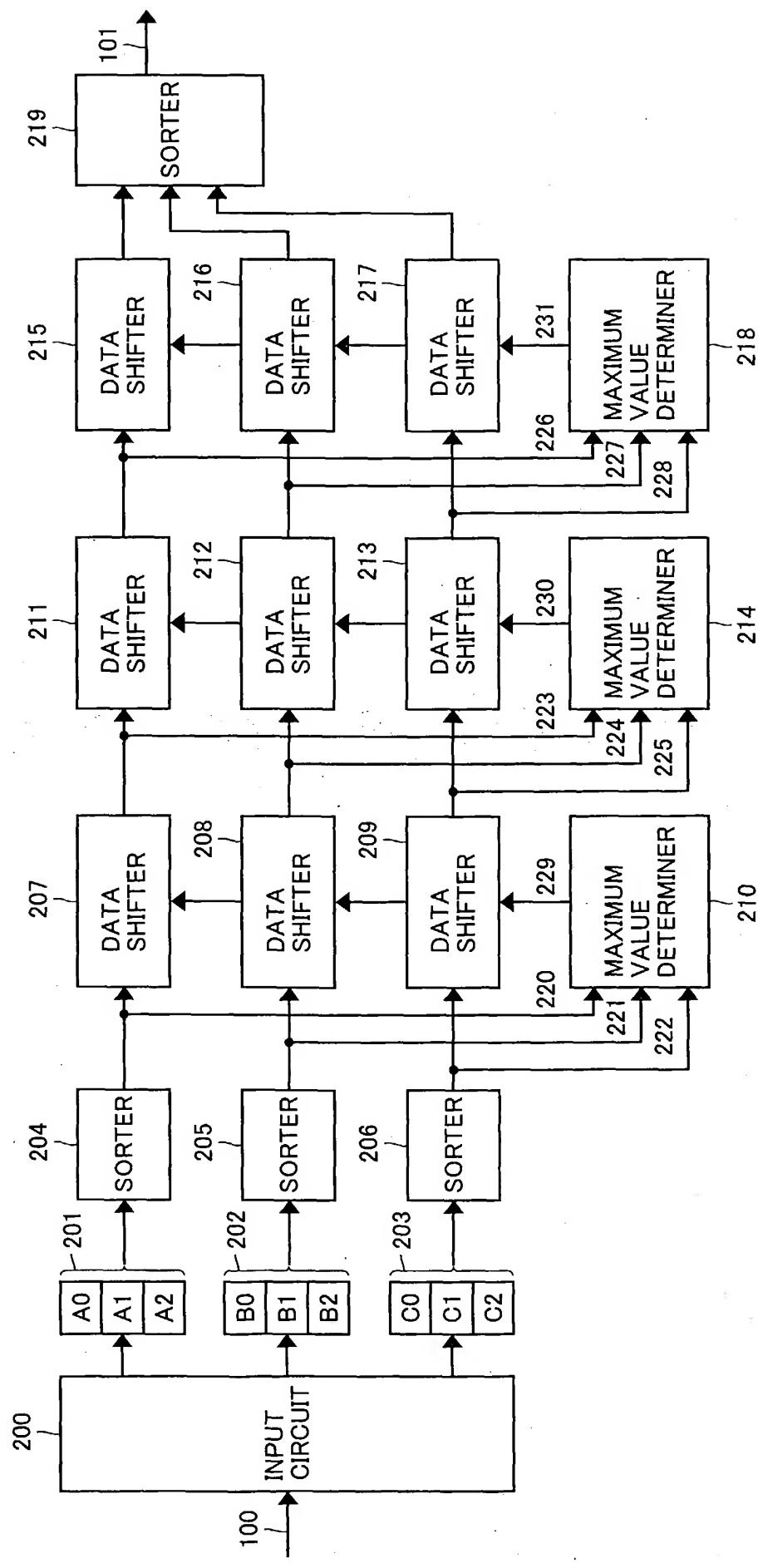


FIG.2A

A0	B0	C0
A1	B1	C1
A2	B2	C2

FIG.2B

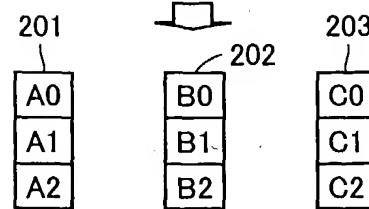


FIG.2C

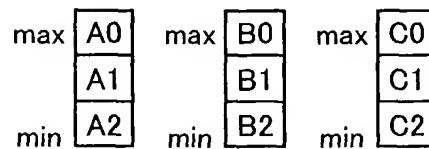


FIG.2D

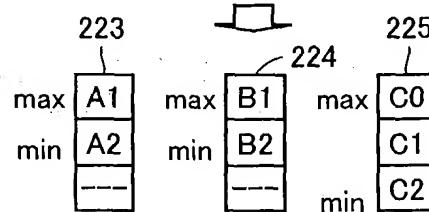


FIG.2E

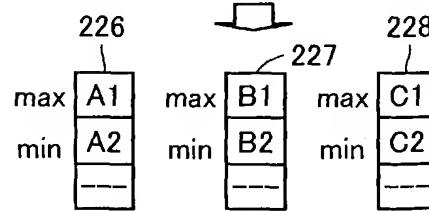


FIG.2F

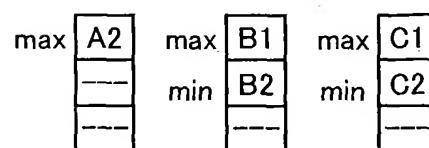


FIG.2G

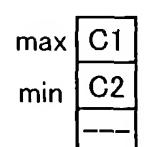


FIG.3

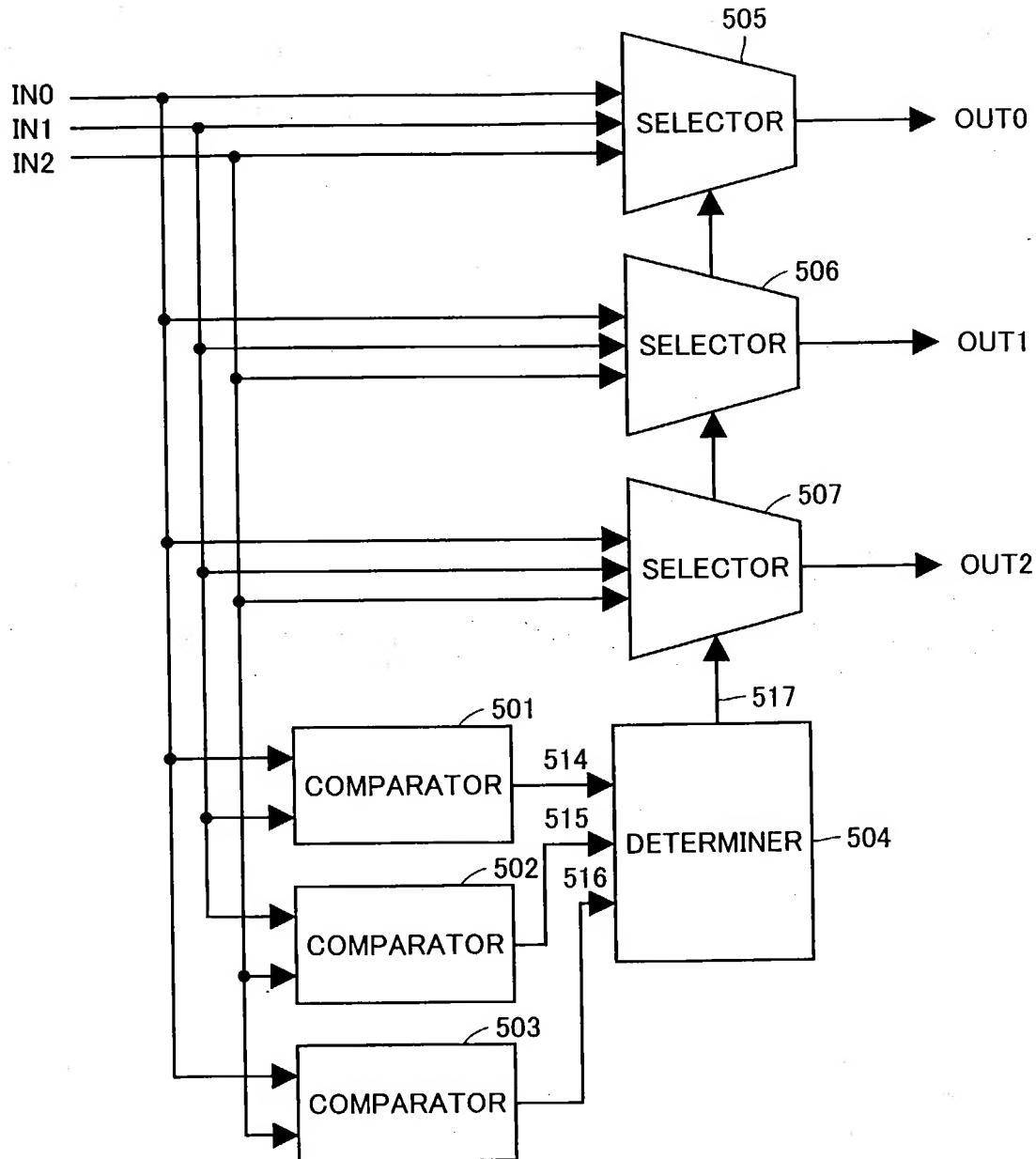


FIG.4

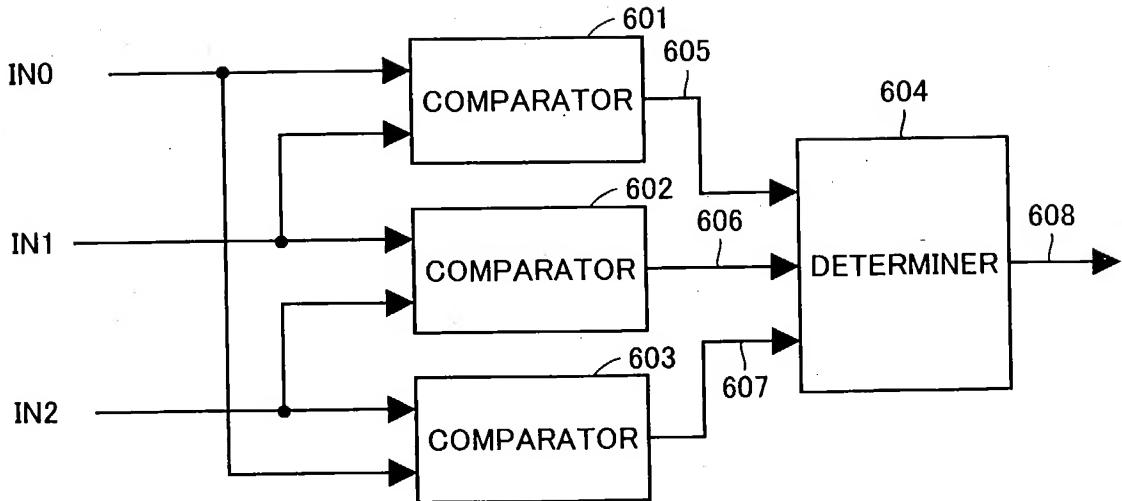


FIG.5

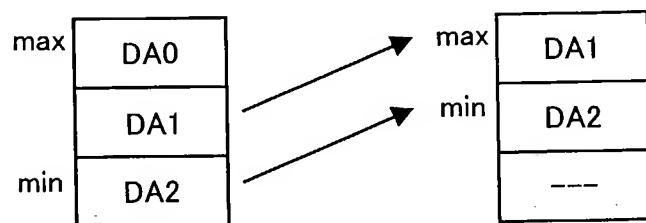


FIG.6A

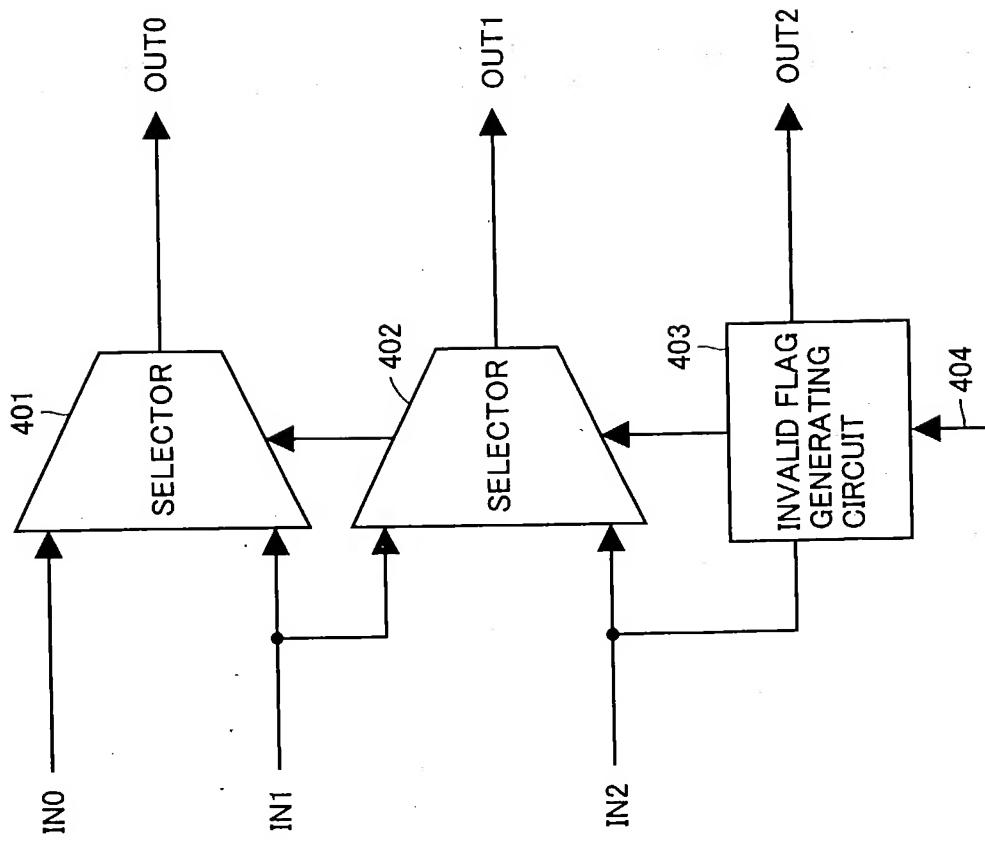


FIG.6B

404: SHIFT SIGNAL	
OUTPUT	ON
OUT0	OFF
OUT0	IN1
OUT1	IN2
OUT2	INVALID
	IN2

FIG. 7

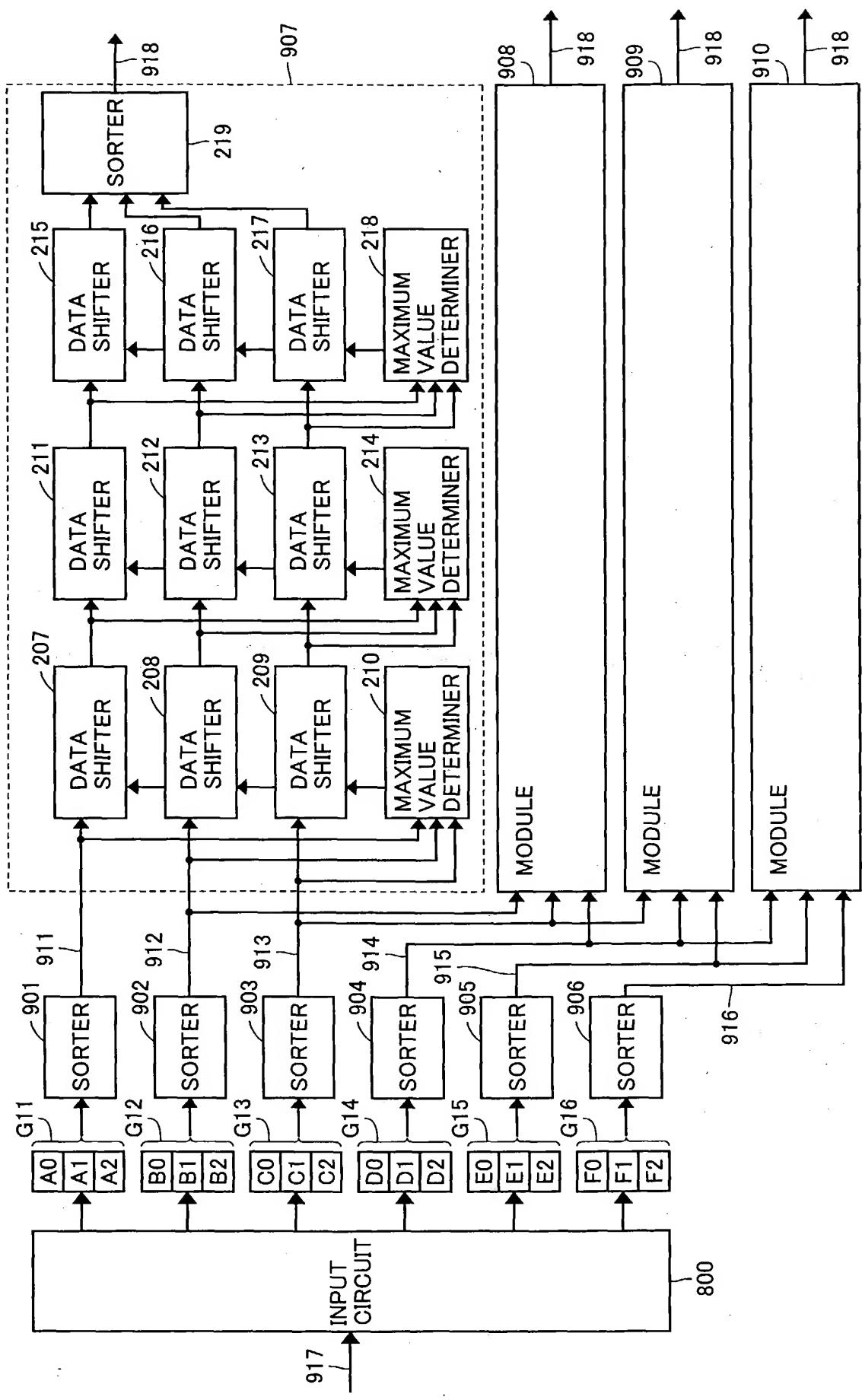


FIG.8

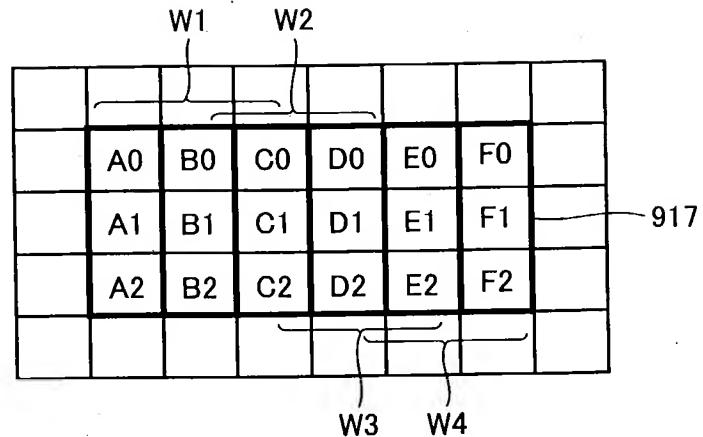


FIG.9

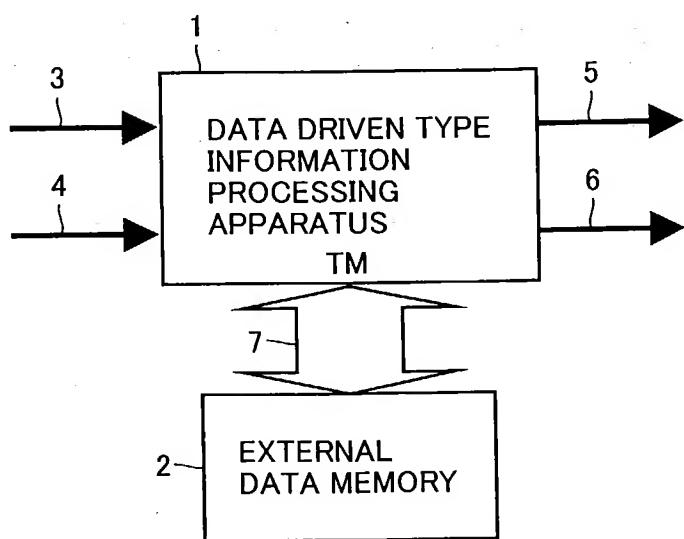


FIG.10

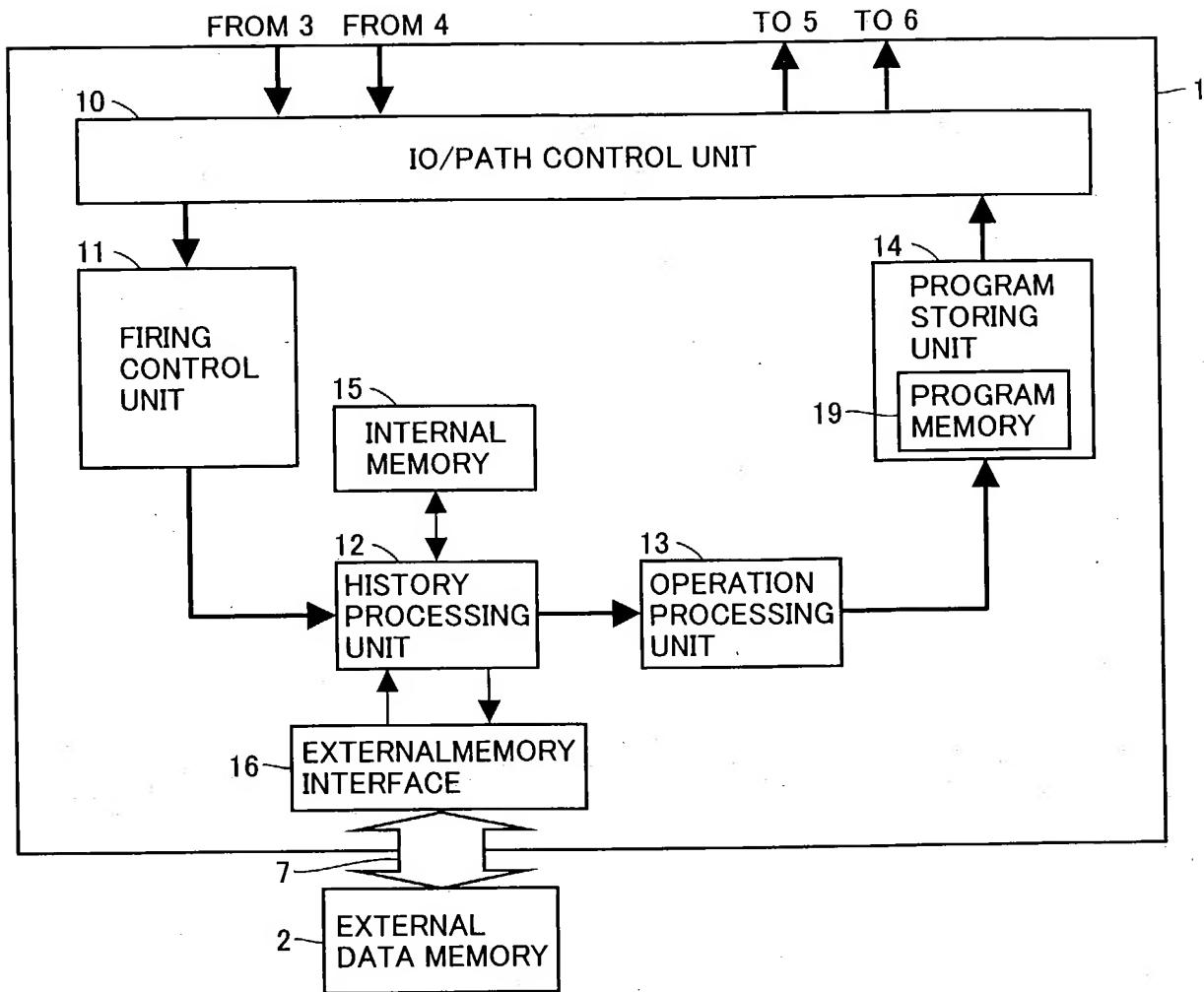
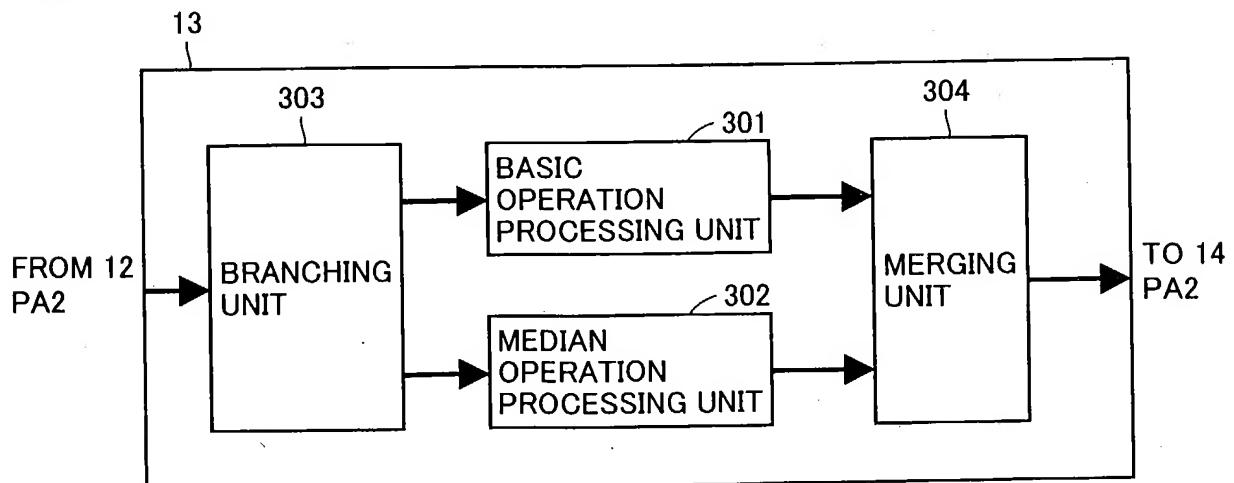


FIG.11



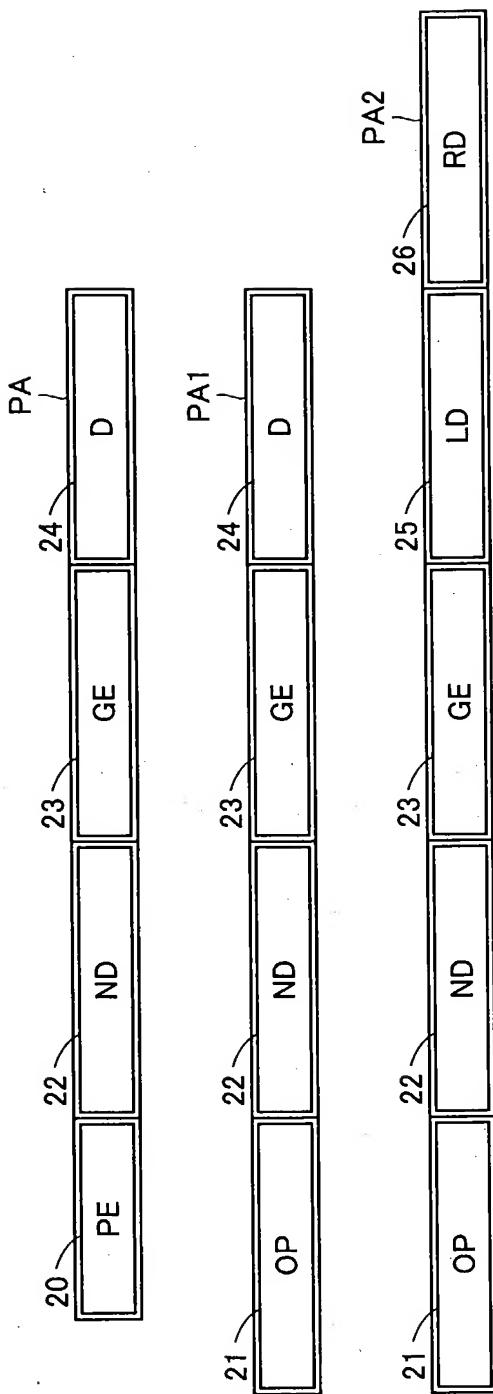


FIG.13A

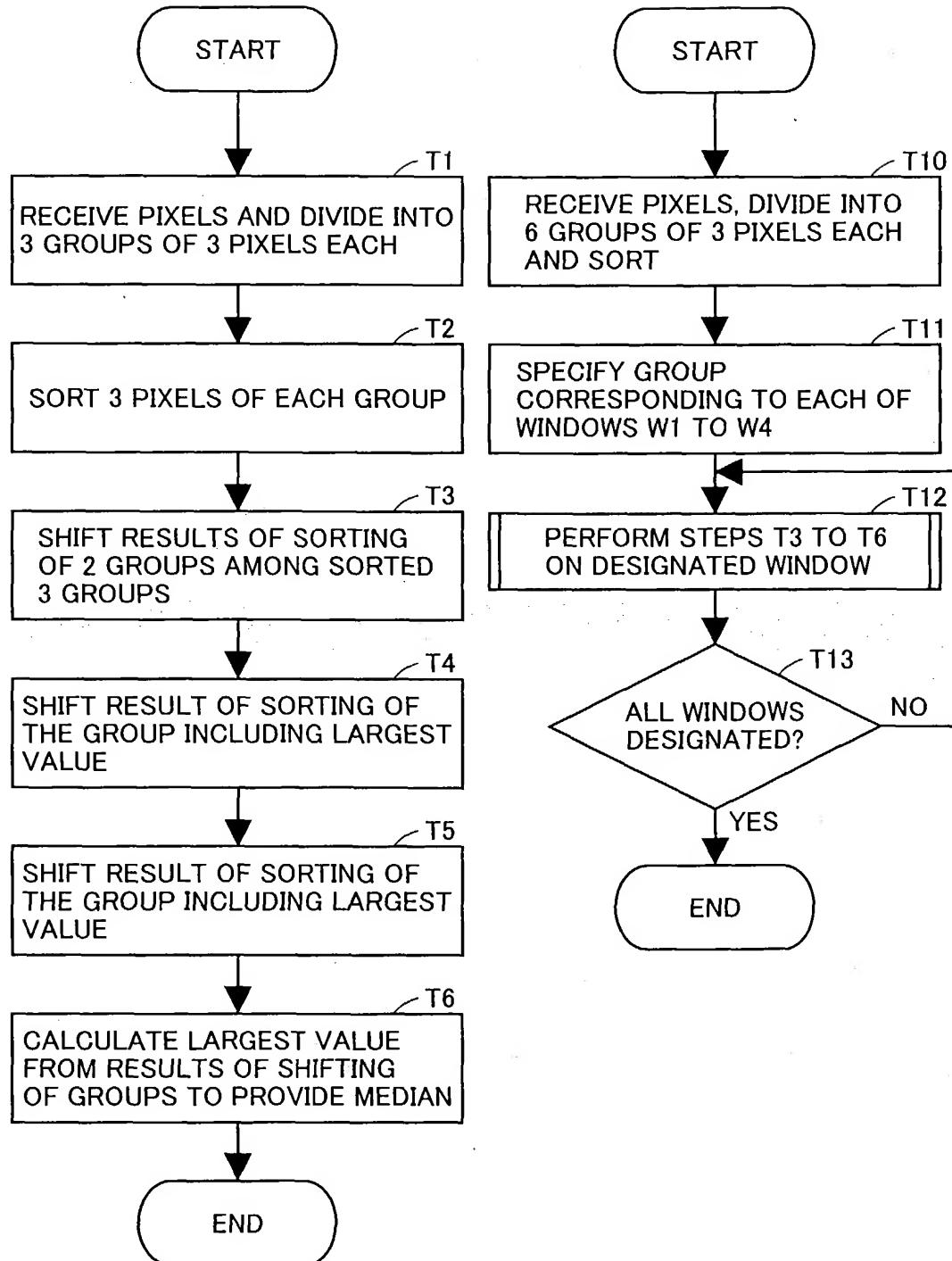


FIG.13B

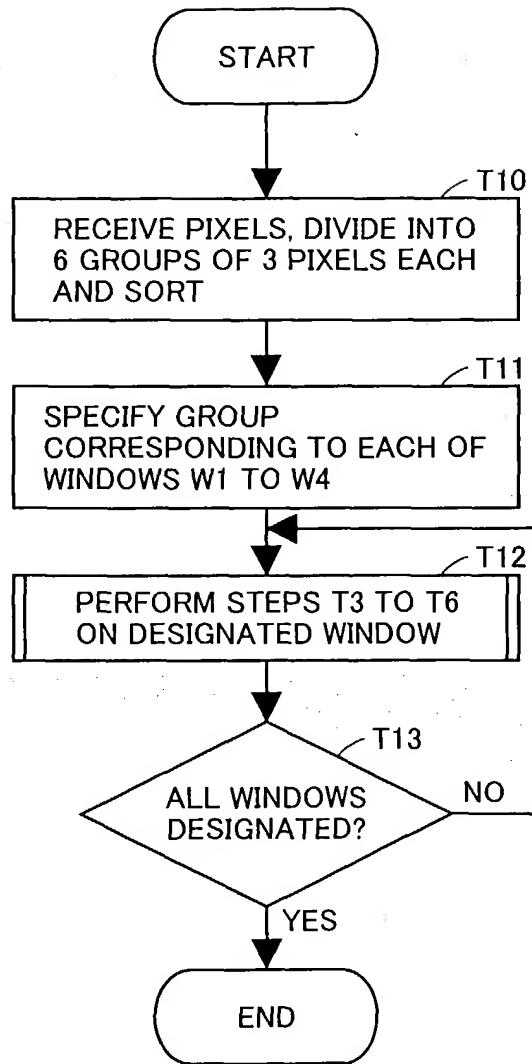


FIG.14

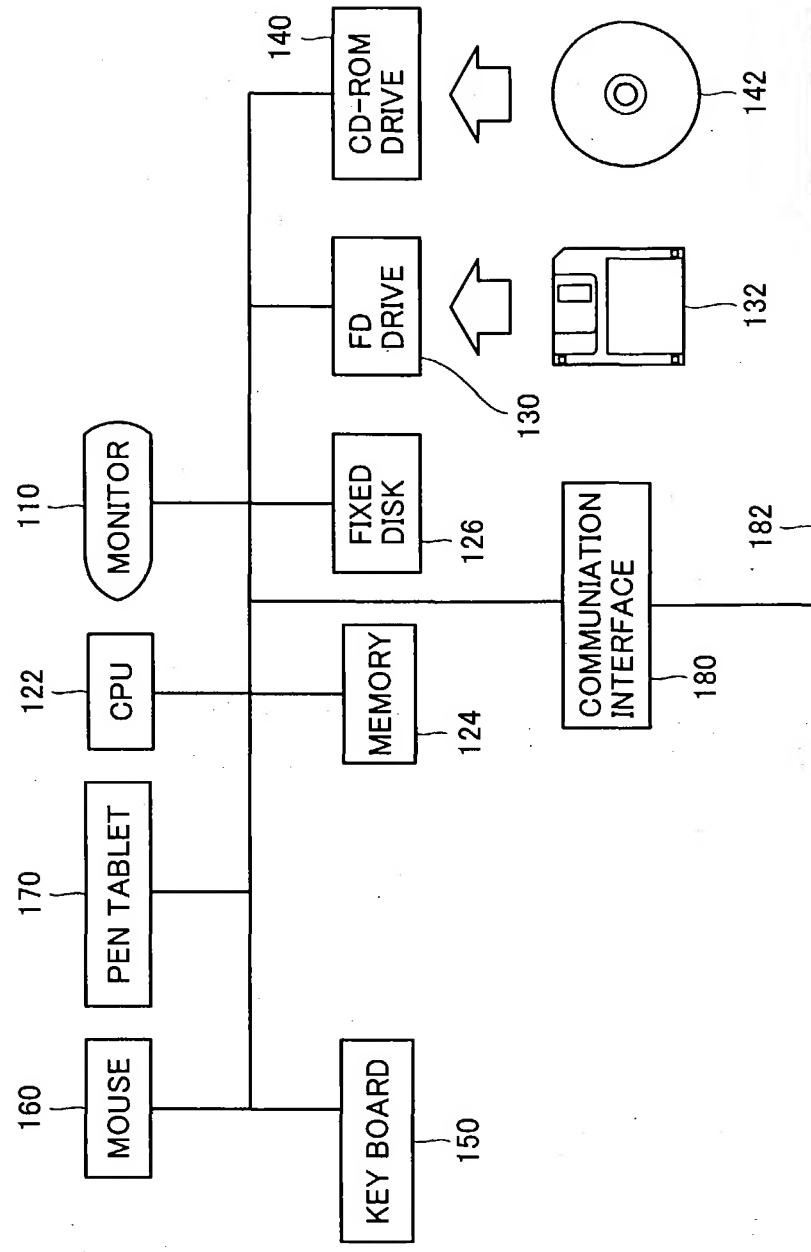


FIG.15 PRIOR ART

